DS1104

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Contents

Chapter 1

Introduction

This document describes a reverse engineered programing interface of the dSpace DS1104 boards. Some information may be inaccurate.

The DC1104 card uses a Motorola MPC8240 CPU. The processor have a PCI interface and works in the agent mode. The board has 32 MiB RAM and 8 MiB ROM. The board have two 4-channel 16-bit DACs and four 12-bit ADCs and one 16-bit ADC with 4-channel multiplexer. The board provides also 20 GPIO pins.

The DS1104 firmware uses Motorola MPC8240 in the big-endian mode. However some registers, especially visible from the PCI bus (such as IDBR) use little-endian byte order. The dSPACE FPGA hardware uses big-endian byte order. However little-endian bit order is used. In description of each register the byte and bit order is defined.

The meaning of the most reserved bits is unknown. Except for the Control Register (4.13) it is safe to write zeros for such bits. The read value is however in most cases random and should be ignored.

1.1 Copyright

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Chapter 2

Functional description

The dSPACE DS1104 card have 32 MiB of Random Access Memory mapped at address `0x00000000`. The RAM is already configured by the card's firmware. The MPC8240 has access to the system PCI bus and to the I/O subsystem. The I/O subsystem is connected via custom FPGA chip using the processor ROM/Flash bus mapped at addresses `0xff000000`–`0xff7fffff`.

2.1 GPIO

The dPSACE DS1104 card have 20 General Purpose I/O pins. Each pin be individually configured as an output or an input by the Digital I/O Direction Register (4.18). The individual bits may be read and set by the Digital I/O Data Register (4.17).

2.2 DACs

The dPSACE DS1104 card have two 4 channel BURR-BROWN DAC7644 16-bit DACs. The DAC registers are accessible via DAC 0 Data Register (4.5) to DAC 7 Data Register (4.12). The RST pin is connected to the `DAC_RST` bit in the Control Register (4.13). The `LOADDACS` is driven by the FPGA depending of the state of DAC Trigger (`DAC_TRIGGER_EXT`, `DAC_TRIGGER_EDGE`, `DAC_TRIGGER_MANUAL`) bits of the Control Register (4.13) and the External Trigger Signal and the `DAC_TRIGGER` bit in the Trigger Register (4.16) depending of the selected mode.

2.3 ADCs

The DS1104 board have five ADCs - one 16-bit LTC1608 (ADC0) and four 12-bit LTC1410 (ADC1 to ADC4). The ADC0 works with a 4 channel MAX609 multiplexer.

Each ADCs is visible as a data register ADC 0 Data Register (4.0.1) to ADC 4 Data Register (4.4). Additionally the ADC Ready signal $\overline{\text{RD}}$ from each ADC can be read from the ADC Status Register (4.14). The conversion start signal $\overline{\text{CONVST}}$ is driven the the trigger logic. The external trigger can be selected individually for each ADC by setting the appropriate `ADCx_TRIGGEER_EXT` bit in the Control Register (4.13). The

DAC_TRIGGEER_EXT	DAC_TRIGGER_EDGE	DAC_TRIGGER_MANUAL	Description
0	-	0	LOADDACS issued automatically during DAC Data Register write
0	-	1	LOADDACS issued by writing 1 to the DAC_TRIGGER bit in the Trigger Register (4.16)
1	0	-	LOADDACS issued on the falling edge of the External Trigger signal
1	1	-	LOADDACS issued on the rising edge of the External Trigger signal

edge of the external trigger that starts the conversion is selected for all ADCs using a ADC_TRIGGER_EDGE bit of the Control Register (4.13).

ADCx_TRIGGEER_EXT	ADC_TRIGGER_EDGE	Description
0	-	ADC Conversion started by writing 1 to the ADCx_TRIGGER bit in the Trigger Register (4.16)
1	0	ADC conversion started on the falling edge of the External Trigger signal
1	1	ADC conversion started on the rising edge of the External Trigger signal

The MAX609 multiplexer is controlled by the ADC 0 Multiplexer Register (4.15).

Chapter 3

Boot

The card has a bootloader in the ROM. It configures the SDRAM and probably does many other thinks. The most important functionality is the Machine Check Exception handler, which can be called using I2O Message interface from a PCI bus.

3.1 IDBR Register

Offset	0x0068
Width	32 bit
Type	RW
Byte order	Little-endian
Bit order	Little-endian
Reset value	—

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCE	Reserved					RUN	STOP	Reserved							
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

IDBR Register Bit Descriptions

Bit	Name	Description
31	MCE	**Machine Check Exception**. Writing this bit as 1 requests Machine Check Exception on the MPC8240 processor. The Machine Check Exception handler provided by the firmware checks for RUN and STOP bits. This bit is cleared by the MCE handler.
30–26	Reserved	**Reserved**. Should be written as 0.
25	RUN	**Run**. Writing this bit as 1 requests execution of the code starting at physical address 0x00000100 if the Boot signature is set. This bit takes precedence over the STOP bit. This bit is cleared by the MCE handler.
24	STOP	**Stop Execution**. Writing this bit as 1 requests stopping the code execution on the MPC8240 processor. The processor returns to an infinite loop, unless the RUN bit was set. This bit is cleared by the MCE handler.
23–0	Reserved	**Reserved**. Should be written as 0.

3.2 Boot signature

To verify that a valid code was provided the card's firmware checks for boot signature.

To execute code on a DS1104 board the user must set following string at address 0x01ff0460:

```
EsistimmerdieHW!
```

Chapter 4

Register descriptions

Runtime Register Summary

Offset	Type	Register	Description
0xff000000	RO	ADC 0 Data Register	4.0.1
0xff000008	RO	ADC 1 Data Register	4.1
0xff000010	RO	ADC 2 Data Register	4.2
0xff000018	RO	ADC 3 Data Register	4.3
0xff000020	RO	ADC 4 Data Register	4.4
0xff080000	RW	DAC 0 Data Register	4.5
0xff080008	RW	DAC 1 Data Register	4.6
0xff080010	RW	DAC 2 Data Register	4.7
0xff080018	RW	DAC 3 Data Register	4.8
0xff080020	RW	DAC 4 Data Register	4.9
0xff080028	RW	DAC 5 Data Register	4.10
0xff080030	RW	DAC 6 Data Register	4.11
0xff080038	RW	DAC 7 Data Register	4.12
0xff300000	RW	Control Register	4.13
0xff300008	RW	ADC Status Register	4.14
0xff300010	RW	ADC 0 Multiplexer Register	4.15
0xff300018	RW	Digital I/O Data Register	4.17
0xff300020	RW	Digital I/O Direction Register	4.18
0xff300038	RW	I/O Trigger Register	4.16

4.0.1 ADC 0 Data Register

Address	0xff000000
Width	32 bit
Type	RO
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	Reserved	**Reserved**. Read value should be ignored.
15–0	Value	**ADC 0 Value**. The Value field returns the output code word from the LTC1608 ADC. It's a 16-bit two's-complement signed value.

4.1 ADC 1 Data Register

Address	0xff000008
Width	32 bit
Type	RO
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved0															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value												Reserved1			
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ADC 1 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–4	`Value`	**ADC 1 Value**. The `Value` field returns the output code word from the LTC1410 ADC. It's a 12-bit two's-complement signed value.
3-0	`Reserved1`	**Reserved**. Read value should be ignored.

4.2 ADC 2 Data Register

Address	`0xff000010`
Width	32 bit
Type	RO
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
`Reserved0`															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
`Value`												`Reserved1`			
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ADC 2 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–4	`Value`	**ADC 2 Value**. The `Value` field returns the output code word from the LTC1410 ADC. It's a 12-bit two's-complement signed value.
3-0	`Reserved1`	**Reserved**. Read value should be ignored.

4.3 ADC 3 Data Register

Address	`0xff000018`
Width	32 bit
Type	RO
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved0															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value												Reserved1			
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ADC 3 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–4	`Value`	**ADC 3 Value**. The `Value` field returns the output code word from the LTC1410 ADC. It's a 12-bit two's-complement signed value.
3-0	`Reserved1`	**Reserved**. Read value should be ignored.

4.4 ADC 4 Data Register

Address	`0xff000020`
Width	32 bit
Type	RO
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved0															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value												Reserved1			
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ADC 4 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–4	`Value`	**ADC 4 Value**. The `Value` field returns the output code word from the LTC1410 ADC. It's a 12-bit two's-complement signed value.
3-0	`Reserved1`	**Reserved**. Read value should be ignored.

4.5 DAC 0 Data Register

Address	`0xff080000`
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
`Reserved`															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
`Value`															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 0 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.6 DAC 1 Data Register

Address	`0xff080008`
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
`Reserved`															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
`Value`															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 1 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.7 DAC 2 Data Register

Address	`0xff080010`
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
`Reserved`															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
`Value`															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 2 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.8 DAC 3 Data Register

Address	`0xff080018`
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 3 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.9 DAC 4 Data Register

Address	`0xff080020`
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 4 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.10 DAC 5 Data Register

Address	0xff080028
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 5 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.11 DAC 6 Data Register

Address	0xff080030
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 6 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.12 DAC 7 Data Register

Address	`0xff080038`
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
`Reserved`															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
`Value`															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ADC 0 Data Register Bit Descriptions

Bit	Name	Description
31–16	`Reserved`	**Reserved**. Read value should be ignored.
15–0	`Value`	**DAC 7 Value**. Write sets the DAC Output register of the DAC7644 DAC. Read reds the value of the DAC Output Register. The `Value` field uses 16-bit unsigned encoding with 32768 offset. The value 0 specifies the minimal DAC output voltage equal to −10 V, the value 32768 represents the 0 V and the 65535 represents the maximal DAC output.

4.13 Control Register

Address	`0xff300000`
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved 31	Reserved 30	Reserved 29	Reserved 28	Reserved 27	Reserved 26	Reserved 25	Reserved 24	Reserved 23	Reserved 22	Reserved 21	Reserved 20	Reserved 19	DAC_TRIGGER_EDGE	DAC_TRIGGER_MANUAL	Reserved 16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved 15	DAC_TRIGGER_EXT	ADC4_TRIGGER_EXT	ADC3_TRIGGER_EXT	ADC2_TRIGGER_EXT	ADC1_TRIGGER_EXT	ADC0_TRIGGER_EXT	ADC_TRIGGER_EDGE	Reserved 7	Reserved 6	Reserved 5	Reserved 4	Reserved 3	Reserved 2	DAC_RST	Reserved 0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Control Register Bit Descriptions

Bit	Name	Description
31–0	Reserved n	**Reserved bit n**. The value should not be modified, use Read-Modify-Write.
18	DAC_TRIGGER_EDGE	**DAC Trigger Rising Edge**. Setting this bit to 1 enables using the rising edge of the External Trigger for triggering DACs. Otherwise the falling edge is used.
17	DAC_TRIGGER_MANUAL	**DAC Trigger Manual**. Setting this bit to 1 enables the manual control of the DAC trigger. This mode requires clearing the DAC_TRIGGER_EXT bit.
14	DAC_TRIGGER_EXT	**DAC External Trigger**. Setting this bit to 1 enables the External Trigger for both DACs. Otherwise the External Trigger is ignored.
13	ADC4_TRIGGER_EXT	**ADC 4 External Trigger**. Setting this bit to 1 enables the External Trigger for the ADC 4. Otherwise the External Trigger is ignored.
12	ADC3_TRIGGER_EXT	**ADC 3 External Trigger**. Setting this bit to 1 enables the External Trigger for the ADC 3. Otherwise the External Trigger is ignored.
11	ADC2_TRIGGER_EXT	**ADC 2 External Trigger**. Setting this bit to 1 enables the External Trigger for the ADC 2. Otherwise the External Trigger is ignored.
10	ADC1_TRIGGER_EXT	**ADC 1 External Trigger**. Setting this bit to 1 enables the External Trigger for the ADC 1. Otherwise the External Trigger is ignored.
9	ADC0_TRIGGER_EXT	**ADC 0 External Trigger**. Setting this bit to 1 enables the External Trigger for the ADC 0. Otherwise the External Trigger is ignored.
8	ADC_TRIGGER_EDGE	**ADC Trigger Rising Edge**. Setting this bit to 1 enables using the rising edge of the External Trigger for triggering ADCs. Otherwise the falling edge is used.
2	DAC_RST	**DAC Reset**. This field controls the state of the RST pin of both DAC7644 DACs. The reset is level triggered and the 1 is the active state. During reset this pin should be set and during normal operation this bit should be cleared. See DAC7644 Datasheet for detailed description.

4.14 ADC Status Register

Address	0xff300008
Width	32 bit
Type	RO
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved 15	Reserved 14	Reserved 13	Reserved 12	Reserved 11	Reserved 10	Reserved 9	Reserved 8	Reserved 7	Reserved 6	Reserved 5	ADC4_BUSY	ADC3_BUSY	ADC2_BUSY	ADC1_BUSY	ADC0_BUSY
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Control Register Bit Descriptions

Bit	Name	Description
31–5	Reserved n	**Reserved bit n**. Read value should be ignored.
4	ADC4_BUSY	**ADC 4 Busy**. The value 1 in this bit indicates that ADC 4 is performing a conversion. The bit is cleared otherwise. It is a value of the $\overline{\text{RD}}$ signal from the LTC1410 ADC 4.
3	ADC3_BUSY	**ADC 3 Busy**. The value 1 in this bit indicates that ADC 3 is performing a conversion. The bit is cleared otherwise. It is a value of the $\overline{\text{RD}}$ signal from the LTC1410 ADC 3.
2	ADC2_BUSY	**ADC 2 Busy**. The value 1 in this bit indicates that ADC 2 is performing a conversion. The bit is cleared otherwise. It is a value of the $\overline{\text{RD}}$ signal from the LTC1410 ADC 2.
1	ADC1_BUSY	**ADC 1 Busy**. The value 1 in this bit indicates that ADC 1 is performing a conversion. The bit is cleared otherwise. It is a value of the $\overline{\text{RD}}$ signal from the LTC1410 ADC 1.
0	ADC0_BUSY	**ADC 0 Busy**. The value 1 in this bit indicates that ADC 0 is performing a conversion. The bit is cleared otherwise. It is a value of the $\overline{\text{RD}}$ signal from the LTC1608 ADC.

4.15 ADC 0 Multiplexer Register

Address	0xff300010
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														CHANNEL	
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW

Control Register Bit Descriptions

Bit	Name	Description
31–2	Reserved	**Reserved bit n**. Should be written as 0. Read value should be ignored.
1-0	CHANNEL	**ADC 0 Channel Selection**. The value sets the selected channel on the ADC 0. The output is connected to the address bits of the MAX309 multiplexer. The output settles after 1 μs after selection of a channel.

4.16 Trigger Register

Address	0xff300038
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved 15	Reserved 14	Reserved 13	Reserved 12	Reserved 11	Reserved 10	Reserved 9	Reserved 8	Reserved 7	Reserved 6	DAC_TRIGGER	ADC4_TRIGGER	ADC3_TRIGGER	ADC2_TRIGGER	ADC1_TRIGGER	ADC0_TRIGGER
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Trigger Register Bit Descriptions

Bit	Name	Description
31–6	`Reserved n`	**Reserved bit n**. Should be written as 0. Read value should be ignored.
5	`DAC_TRIGGER`	**DAC Trigger**. Writing 1 to this bit updates all DAC Outputs. The LOADDACS pulse is issued on both DACs. This operation should be used when the manual trigger DAC mode is set.
4	`ADC4_TRIGGER`	**ADC 4 Trigger**. Writing 1 to this bit triggers a conversion on the ADC 4.
3	`ADC3_TRIGGER`	**ADC 3 Trigger**. Writing 1 to this bit triggers a conversion on the ADC 3.
2	`ADC2_TRIGGER`	**ADC 2 Trigger**. Writing 1 to this bit triggers a conversion on the ADC 2.
1	`ADC1_TRIGGER`	**ADC 1 Trigger**. Writing 1 to this bit triggers a conversion on the ADC 1.
0	`ADC0_TRIGGER`	**ADC 0 Trigger**. Writing 1 to this bit triggers a conversion on the ADC 0. If the ADC conversion is started immediately after changing the ADC channel on the multiplexer the result might be inaccurate. At least 1 μs delay should be used.

4.17 Digital I/O Data Register

Offset	0x40
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
`R31`	`R30`	`R29`	`R28`	`R27`	`R26`	`R25`	`R24`	`R23`	`R22`	`R21`	`R20`	`D19`	`D18`	`D17`	`D16`
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
`D15`	`D14`	`D13`	`D12`	`D11`	`D10`	`D9`	`D8`	`D7`	`D6`	`D5`	`D4`	`D3`	`D2`	`D1`	`D0`
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Digital I/O Data Register Bit Descriptions

Bit	Name	Description
31–20	Rn	**Reserved bit n**. Should be written as 0. Read value should be ignored.
19–0	Dn	**Digital I/O pin n value**. The Dn bit shows the logical value of n-th Digital I/O pin. The bit value is equal to 1 if the voltage is applied to digital input; it's equal to 0 otherwise.

4.18 Digital I/O Direction Register

Offset	0x40
Width	32 bit
Type	RW
Byte order	Big-endian
Bit order	Little-endian

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R31	R30	R29	R28	R27	R26	R25	R24	R23	R22	R21	R20	O19	O18	O17	O16
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Digital I/O Direction Register Bit Descriptions

Bit	Name	Description
31–20	Rn	**Reserved bit n**. Should be written as 0. Read value should be ignored.
19–0	On	**Digital I/O pin n direction**. If the On bit is equal to 1 the pin n is configured as an output. The value 0 sets the pin n as an input.